Prototype Trace Probe

and Probe Adapter

Partner: Trinity College Dublin
Author(s): B.A.Coghlan, M.Manzke
Editor: B.A.Coghlan

Keywords: SCI, trace, probe, analysis

Abstract:

In this document we present the technical manual for the prototype trace probe and probe adapter developed within the project.
Contents

Introduction .................................................................................................................. 3

Trace Probe DT204.1 Technical Manual ................................................................. 5
  Features ...................................................................................................................... 6
  Functional Overview .............................................................................................. 7
  Trace Example 1 : Trace from Dolphin’s D310 .................................................... 13
  Trace Example 2 : Trace from SCI cable via SCILab’s SCITrac tracer ............. 16
  Layouts ...................................................................................................................... 19
  Electrical Characteristics ....................................................................................... 22
  Parts List .................................................................................................................. 23
  Patch List ................................................................................................................. 25
  Document History .................................................................................................. 26

Probe Adapter DT205.1 Technical Manual .............................................................. 27
  Features ...................................................................................................................... 28
  Functional Overview .............................................................................................. 29
  Layouts ...................................................................................................................... 33
  Electrical Characteristics ....................................................................................... 36
  Parts List .................................................................................................................. 37
  Patch List ................................................................................................................. 39
  Document History .................................................................................................. 40
ESPRIT Project P25257 SCIEurope

Deliverable D 2.2.1b

Prototype Trace Probe and Probe Adapter

April 1999

Dr. B.A. Coghlan
Department of Computer Science
Trinity College Dublin
coghlan@cs.tcd.ie

M. Manzke
Department of Computer Science
Trinity College Dublin
michael.manzke@cs.tcd.ie
Introduction

The definition of Task 2.2.1 is as follows:

<table>
<thead>
<tr>
<th>Task and User Need</th>
<th>Test Tools Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>Market and User Need</td>
<td>There are no commercially available SCI test tools on the market for the SCI community today.</td>
</tr>
<tr>
<td>Objectives</td>
<td>To develop the first generation of tracing and debugging tools for use in work package 3 Applications.</td>
</tr>
<tr>
<td>Approach</td>
<td>The tools will be based on needs identified in the Test Requirements Specification from Task 2.1. There will probably be developed two tools – one tool able to trace the SCI traffic and either show online or store the results. This tool will be based as much as possible on present hardware and software platforms. The other tool will be able to send and receive SCI traffic according to some traffic profile in order to load systems with traffic without using real nodes. The prototype tools will be evaluated during the debugging phase of the Embedded Avionics System demonstrator in Task 3.3, and the results will be summarised in a report.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Lead Partner</th>
<th>Trinity</th>
<th>24 person months</th>
</tr>
</thead>
<tbody>
<tr>
<td>Other Partners</td>
<td>D.E. SINTEF</td>
<td>4 person months 12 person months</td>
</tr>
<tr>
<td>Major deliverables</td>
<td>D 2.2.1 Q4 Trinity Prototype Trace/Analyzer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D 2.2.2 Q6 SINTEF Traffic Generation Tool</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D 2.2.3 Q8 Trinity Trace/Analyzer Mk.II</td>
<td></td>
</tr>
</tbody>
</table>

B-Link traces can be acquired via a probe card supplied by Dolphin, that attaches to their SCI cards via elastomeric connectors, and breaks out the B-Link signals to a number of connectors that will accept cables for a HP16500 series logic analyser. Trinity have designed a trace probe and probe adapter that will attach to these to distribute the B-Link signals to a multiple of the DT200.1 Deep Trace boards previously described in Deliverable D2.2.1a.

The objective of this document is to present the Technical Manual for the Prototype Trace Probe and Probe Adapter. These represent the SCI-specific hardware resources of the Prototype Trace/Analyzer.
Trace Probe DT204.1

Technical Manual
Introduction

The DT204.1 Trace Probe is designed for interfacing IEEE 1596 Scalable Coherent Interconnect (SCI) systems to the DT200.1 Deep Tracer, which is a modular data collection system designed specifically for gathering very long state traces for performance analysis of SCI systems. Two trace probes are needed, each to attach via a DT205.1 Probe Adapter to one of the two deep trace boards.

Features

• 96bit tracing
  Max Sample Rate 66MHz.

• Tracing Dolphin’s D310 B-Link
  Attaches to Dolphin Probe Card.

• Tracing SCI cable via SCILab’s SCITrac tracer
  Attaches to SCILab tracer, replacing a logic analyzer.

• Co-ordinated trace of host activity
  16bit header for attaching host tracer.

• Simple deep tracer interface
  34-wire LVDS cable.

• Programmable logic via JTAG
  May be used for test pattern generation or data pattern matching.
Trace Probe Functional Overview

A simplified schematic of the trace probe is shown below.

Each trace probe attaches to 48 bits of a 96bit sample data path. All data signals are parallel terminated by 390 ohms to a reference voltage that is generated by voltage regulator VREG2. One of three reference voltages may be selected via strap J22 as follows:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>J22 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>140mV</td>
<td>none</td>
</tr>
<tr>
<td>220mV</td>
<td>B-A</td>
</tr>
<tr>
<td>TBD</td>
<td>B-C</td>
</tr>
</tbody>
</table>

Six DS92L90A 9 bit LVDS tranceivers are configured to compare the sample data to the selected reference voltage. The comparator outputs are low-voltage TTL. Care is taken to minimize any data skews.

Two trace probes are synchronized via an inter-probe cable that connects to IPCON. Its pinout is as follows:

<table>
<thead>
<tr>
<th>IPCLK</th>
<th>GND</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>IP0</td>
<td>GND</td>
</tr>
<tr>
<td>IP1</td>
<td>GND</td>
</tr>
<tr>
<td>IP2</td>
<td>GND</td>
</tr>
<tr>
<td>IP3</td>
<td>GND</td>
</tr>
<tr>
<td>IP4</td>
<td>GND</td>
</tr>
<tr>
<td>IP5</td>
<td>GND</td>
</tr>
<tr>
<td>IP6</td>
<td>GND</td>
</tr>
<tr>
<td>IP7</td>
<td>TXSYN</td>
</tr>
</tbody>
</table>
Functional Overview

The sample clock may be derived from four different sources: input connectors E1, E2 or EC, or the inter-probe connector IPCON. Three of the the clock sources are selected via J21:

![Diagram of clock selection via J21](image)

<table>
<thead>
<tr>
<th>Clock Source</th>
<th>J21 Straps</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1CLK</td>
<td>E1-CLK</td>
</tr>
<tr>
<td>E2CLK</td>
<td>E2-CLK</td>
</tr>
<tr>
<td>ECCLK</td>
<td>EC-CLK</td>
</tr>
</tbody>
</table>

The unselected clocks may be utilized if specifically desired by strapping them to the MACH445 inputs and programming the MACH445 accordingly. A CDC340 clock driver, CLKDVR, buffers the selected clock to independently drive a number of destinations, including J11, which determines the function of the IPCLK signal at the inter-probe connector IPCON. J11 may be set up to output the selected clock to the other trace probe, or to input a clock from the other trace probe. Care is taken to minimize any clock skews.

![Diagram of IPCLK and J11 straps](image)

<table>
<thead>
<tr>
<th>IPCLK</th>
<th>J11 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPCLK as input to CLKDVR</td>
<td>B-A</td>
</tr>
<tr>
<td>IPCLK as output from CLKDVR</td>
<td>B-C</td>
</tr>
</tbody>
</table>

The data and control fields are treated differently. The data signals from E1 & E2 are pipelined via 74646 registers REG0-3, as well as being fed to a MACH445 pal. The control signals from EC are connected to the J3-10 straps, from which they may be strapped to a further 74646 register REG4 as well as the MACH445 pal, or to the inter-probe connector IPCON as signals IP7-0, see below. Those control signals strapped to the inter-probe connector are pipelined by the matching register REG4 on the other trace probe, which must also derive its clock from the inter-probe connector using the strapping given above.

![Diagram of J3-10 straps](image)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-8 from BUF5</td>
<td>7-0 from BUF4</td>
<td>IP7-0 from IPCON</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Strapblock J3-10
The 74646 registers' direction control input DIR, which is also connected to the DE input of the DS92L90, is resistively pulled down to ground, while their output enable input /G, which is connected to the /RE input of the DS92L90, is resistively pulled up to +3.3V (their SAB and SBA inputs are also resistively pulled up to +3.3V); these connections allow the possibility of using the trace probe to generate synthetic trace data. Both of the above signals connect to and can be driven by the MACH445.

The MACH445 pal also pipelines an 8bit portion of a 16bit external data input from EXTCON that can be connected to any external source, but is intended for connection to a host tracer, such as a VMetro PCI analyzer. Its pinout is:

<table>
<thead>
<tr>
<th>Top</th>
<th>Bottom</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>extCLK</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD0</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD1</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD2</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD3</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD4</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD5</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD6</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD7</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD8</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD9</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD10</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD11</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD12</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD13</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD14</td>
</tr>
<tr>
<td>GND</td>
<td>ExtD15</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

Each trace probe is strapped to trace an appropriate 8bit field of the external data as follows:

<table>
<thead>
<tr>
<th>External Data</th>
<th>Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>extD7-0</td>
<td>J12-19 B-C</td>
</tr>
<tr>
<td>extD15-8</td>
<td>J12-19 B-A</td>
</tr>
</tbody>
</table>

These signals are parallel terminated with 220 ohms to +5V and 330 ohms to ground. The external clock is separately terminated, with 22 ohms in series followed by 220 ohms to +5V and 330 ohms to ground.
The MACH445 pal can also be used as a test pattern generator, deriving its clock from a local crystal oscillator OSC (typically 100MHz), which is buffered by a CDC340 clock driver OSCDVR. It may be programmed via a JTAG interface using the MACHXL software.

The MACH445 pal can further be employed to match specific input data patterns, again programmed via the JTAG interface using the MACHXL software. The match results can be pipelined to the tracer via the control fields. This would also be useful if the host tracer required data input rather than generating output, since pattern matching could be utilized to indicate SCI events to the host tracer by programming the MACH445 to generate event identifiers on the external interface.

Two JTAG connectors are provided. The upstream of the JTAG chain connects to JTAGIN, and the downstream connects to JTAGOUT. Their pin connections are:

<table>
<thead>
<tr>
<th>/ENABLE</th>
<th>/TRST</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>TDO</td>
</tr>
<tr>
<td>TVCC</td>
<td>TDI</td>
</tr>
<tr>
<td>GND</td>
<td>TMS</td>
</tr>
<tr>
<td>ZCTL</td>
<td>TCK</td>
</tr>
</tbody>
</table>

In the event that there is no downstream chain, TDI should be strapped to TDO at connector JTAGOUT. Note that signals /TRST, /ENABLE and TVCC are resistively pulled up to +5V, while signal ZCTL is resistively pulled down to ground.

The MACH445 may be programmed in-circuit, but since it does not program reliably in-circuit if any of its I/O pins are toggling, any signals that drive the MACH445 are disabled with the JTAG /ENABLE signal, and thus the trace probe is unusable while programming.

The pipelined outputs are converted to multiplexed LVDS using two DS90C283 devices, TX1 for the low 24bits, and TX0 for the high 24bits. These devices multiplex a 28bit TTL data path onto a LVDS cable. Since the data from different devices may be skewed (relative to each other) at the end of the LVDS cables, a synchronizing pulse TXSYN is sent over the 25th bit (and over the inter-probe connector as IPSYN); this repeats every 3 clock cycles. The synchronizing pulse is selected as follows:

<table>
<thead>
<tr>
<th>TXSYN</th>
<th>J2 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>MACH445 generates IPSYN</td>
<td>B-C</td>
</tr>
<tr>
<td>IPSYN is an input</td>
<td>-</td>
</tr>
</tbody>
</table>

A 34-way flat cable (typically a floppy-disk cable), carrying eight differential signals plus two differential clocks, connects the LVDS outputs at LVDSCON to the probe adapter at the deep trace board. The pinout is:

<table>
<thead>
<tr>
<th>Left</th>
<th>Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx1CLKP</td>
<td>Tx0CLKP</td>
</tr>
<tr>
<td>AGND</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx1OUT2P</td>
<td>Tx1OUT2M</td>
</tr>
<tr>
<td>AGND</td>
<td>Tx1OUT3P</td>
</tr>
<tr>
<td>Tx1OUT3M</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx1OUT1P</td>
<td>Tx1OUT1M</td>
</tr>
<tr>
<td>AGND</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx1OUT0P</td>
<td>Tx1OUT0M</td>
</tr>
<tr>
<td>N.C.</td>
<td>N.C.</td>
</tr>
<tr>
<td>Tx0CLKP</td>
<td>Tx0CLKM</td>
</tr>
<tr>
<td>AGND</td>
<td>AGND</td>
</tr>
</tbody>
</table>
The pipelined outputs are also connected to two 40-way flat cable connectors, NSCON0 for the low 24bits, and NSCON1 for the high 24bits. These are intended both for debugging and for connection to the National Semiconductor LVDS demo hardware, and would not normally be used. Their pinout is:

<table>
<thead>
<tr>
<th>signal</th>
<th>pin no.</th>
<th>pin no.</th>
<th>signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>1</td>
<td>2</td>
<td>SAFE12V</td>
</tr>
<tr>
<td>VEESAFE</td>
<td>3</td>
<td>4</td>
<td>VEEADJ</td>
</tr>
<tr>
<td>EBABLK</td>
<td>5</td>
<td>6</td>
<td>GND</td>
</tr>
<tr>
<td>M</td>
<td>7</td>
<td>8</td>
<td>DE</td>
</tr>
<tr>
<td>GND</td>
<td>9</td>
<td>10</td>
<td>LP(HSYNC)</td>
</tr>
<tr>
<td>FLM(VSTNC)</td>
<td>11</td>
<td>12</td>
<td>GND</td>
</tr>
<tr>
<td>SHFCLK</td>
<td>13</td>
<td>14</td>
<td>GND</td>
</tr>
<tr>
<td>P0</td>
<td>15</td>
<td>16</td>
<td>P1</td>
</tr>
<tr>
<td>GND</td>
<td>17</td>
<td>18</td>
<td>P2</td>
</tr>
<tr>
<td>P3</td>
<td>19</td>
<td>20</td>
<td>GND</td>
</tr>
<tr>
<td>P4</td>
<td>21</td>
<td>22</td>
<td>P5</td>
</tr>
<tr>
<td>GND</td>
<td>23</td>
<td>24</td>
<td>P6</td>
</tr>
<tr>
<td>P7</td>
<td>25</td>
<td>26</td>
<td>GND</td>
</tr>
<tr>
<td>P8</td>
<td>27</td>
<td>28</td>
<td>P9</td>
</tr>
<tr>
<td>GND</td>
<td>29</td>
<td>30</td>
<td>P10</td>
</tr>
<tr>
<td>P11</td>
<td>31</td>
<td>32</td>
<td>GND</td>
</tr>
<tr>
<td>P12</td>
<td>33</td>
<td>34</td>
<td>P13</td>
</tr>
<tr>
<td>GND</td>
<td>35</td>
<td>36</td>
<td>P14</td>
</tr>
<tr>
<td>P15</td>
<td>37</td>
<td>38</td>
<td>GND</td>
</tr>
<tr>
<td>P16</td>
<td>39</td>
<td>40</td>
<td>P17</td>
</tr>
<tr>
<td>GND</td>
<td>41</td>
<td>42</td>
<td>P18</td>
</tr>
<tr>
<td>P19</td>
<td>43</td>
<td>44</td>
<td>GND</td>
</tr>
<tr>
<td>P20</td>
<td>45</td>
<td>46</td>
<td>P21</td>
</tr>
<tr>
<td>GND</td>
<td>47</td>
<td>48</td>
<td>P22</td>
</tr>
<tr>
<td>P23</td>
<td>49</td>
<td>50</td>
<td>GND</td>
</tr>
</tbody>
</table>

5V power is normally obtained from PWRCON0, or alternatively from PWRCON1. An LED, PWRLED, indicates when power is present. A 3.3V voltage regulator, VREG1, then generates 3.3V for those devices that need it. There are four internal PCB power planes: +5V, +3.3V, digital ground and analog ground. A substantial reference voltage area approximates a fifth internal power plane. The DS92L90 devices have isolated power and grounds for their LVDS interfaces; power is isolated via filters while ground is isolated via an approximation to single-point connection of the analog ground plane.
Functional Overview

The DS9C283 devices also have isolated power and grounds for both the LVDS interfaces and their phase-lock loops; power is isolated via filters while ground is isolated via trace inductances.

Either a 3.3V or a 5V MACH445 pal can be used, but the appropriate supply voltage must be selected via J20:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>J20 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>B-A</td>
</tr>
<tr>
<td>5V</td>
<td>B-C</td>
</tr>
</tbody>
</table>

Strap J1 can be shorted to power down the DS90C283 devices.
Trace Example 1: Trace from Dolphin’s D310 B-Link

A Dolphin probe card must first be attached to the D310. Two DT204.1 trace probes can be attached to the Dolphin probe card as follows:

1. Trace probe 0:
   - E1 connects to probe card E1
   - E2 connects to probe card E2
   - EC connects to probe card E5
2. Trace probe 1:
   - E1 connects to probe card E3
   - E2 connects to probe card E4
   - EC connects to probe card E6
3. An inter-probe cable must interconnect IPCON of trace probes 0 & 1.
4. The upstream JTAG daisy chain should be connected to JTAGIN of trace probe 0. A JTAG cable should interconnect JTAGOUT of trace probe 0 to JTAGIN of trace probe 1. The downstream chain should be connected to JTAGOUT of trace probe 1, but in the event of there being no downstream chain, its TDI should be strapped to its TDO.
5. Trace probes 0 & 1 must be connected via a DT205.1 probe adapter to deep trace board 0 & 1, respectively.
6. A synchronizing cable must interconnect J6 of probe adapters 0 & 1, respectively.
7. A trigger/trace cable must interconnect EXTCON of deep trace boards 0 & 1, respectively.

Then the straps must be selected as follows.

8. For both trace probes, the reference voltage must be selected via strap J22:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>J22 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>140mV</td>
<td>none</td>
</tr>
</tbody>
</table>

9. For trace probe 0, E1 must be selected as the clock source, and the IPCLK signal must be set up to output the selected clock to the other trace probe:

<table>
<thead>
<tr>
<th>Clock Source</th>
<th>J21 Straps</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1</td>
<td>E1-OUT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IPCLK</th>
<th>J11 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPCLK as output from CLKDVR</td>
<td>B-C</td>
</tr>
</tbody>
</table>

10. For trace probe 1, the clock source must come from IPCLK rather than E1, and the IPCLK signal must be set up to input the selected clock from the other trace probe:
11. For trace probe 0, the C7-0 must be strapped to register REG4, and C15-8 must be strapped to the inter-probe connector:

```
<table>
<thead>
<tr>
<th>Control Signals</th>
<th>Register Strap</th>
<th>Inter-probe Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>C7-0 to register</td>
<td>J3-10 C-D</td>
<td></td>
</tr>
<tr>
<td>C15-8 to IP7-0</td>
<td></td>
<td>J3-10 B-E</td>
</tr>
</tbody>
</table>
```

12. For trace probe 1, the IP7-0 must be strapped to the register:

```
<table>
<thead>
<tr>
<th>Control Signals</th>
<th>Register Strap</th>
<th>Inter-probe Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP7-0 to register</td>
<td></td>
<td>J3-10 A-B</td>
</tr>
</tbody>
</table>
```

13. Each trace probe is strapped to trace an appropriate 8bit field of the external data as follows:

```
<table>
<thead>
<tr>
<th>External Data</th>
<th>Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>extD7-0</td>
<td>J12-19 B-C</td>
</tr>
<tr>
<td>extD15-8</td>
<td>J12-19 B-A</td>
</tr>
</tbody>
</table>
```

14. For trace probe 0, TXSYN must be output to the inter-probe connector:

```
<table>
<thead>
<tr>
<th>TXSYN</th>
<th>J2 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>MACH445 generates IPSYN</td>
<td>B-C</td>
</tr>
</tbody>
</table>
```

15. For trace probe 1, IPSYN must be treated as an input:

```
<table>
<thead>
<tr>
<th>TXSYN</th>
<th>J2 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPSYN is an input</td>
<td>-</td>
</tr>
</tbody>
</table>
```

The aggregated sample data fields are then as follows:
### Functional Overview

<table>
<thead>
<tr>
<th>SDxx</th>
<th>SCLOCK</th>
<th>DT200 board 0</th>
<th>DT200 board 1</th>
<th>MACH445 board 0</th>
<th>MACH445 board 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>bclk</td>
<td>bclk</td>
<td>i0/clk0</td>
<td>i0/clk0</td>
</tr>
<tr>
<td>0</td>
<td>d0</td>
<td>d32</td>
<td>8</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>d1</td>
<td>d33</td>
<td>9</td>
<td>i1/clk1</td>
<td>oscout</td>
</tr>
<tr>
<td>2</td>
<td>d2</td>
<td>d34</td>
<td>10</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>d3</td>
<td>d35</td>
<td>11</td>
<td>i2</td>
<td>extclk</td>
</tr>
<tr>
<td>4</td>
<td>d4</td>
<td>d36</td>
<td>12</td>
<td>i3/clk2</td>
<td>extclk</td>
</tr>
<tr>
<td>5</td>
<td>d5</td>
<td>d37</td>
<td>13</td>
<td>i4/clk3</td>
<td>extclk</td>
</tr>
<tr>
<td>6</td>
<td>d6</td>
<td>d38</td>
<td>14</td>
<td>i5</td>
<td>extclk</td>
</tr>
<tr>
<td>7</td>
<td>d7</td>
<td>d39</td>
<td>15</td>
<td>40</td>
<td>bufre</td>
</tr>
<tr>
<td>8</td>
<td>d8</td>
<td>d40</td>
<td>16</td>
<td>41</td>
<td>bufre</td>
</tr>
<tr>
<td>9</td>
<td>d9</td>
<td>d41</td>
<td>17</td>
<td>42</td>
<td>(userr)</td>
</tr>
<tr>
<td>10</td>
<td>d10</td>
<td>d42</td>
<td>18</td>
<td>43</td>
<td>(attn)</td>
</tr>
<tr>
<td>11</td>
<td>d11</td>
<td>d43</td>
<td>19</td>
<td>44</td>
<td>(int0)</td>
</tr>
<tr>
<td>12</td>
<td>d12</td>
<td>d44</td>
<td>20</td>
<td>45</td>
<td>(obs0)</td>
</tr>
<tr>
<td>13</td>
<td>d13</td>
<td>d45</td>
<td>21</td>
<td>46</td>
<td>(int1)</td>
</tr>
<tr>
<td>14</td>
<td>d14</td>
<td>d46</td>
<td>22</td>
<td>47</td>
<td>(obs1)</td>
</tr>
<tr>
<td>15</td>
<td>d15</td>
<td>d47</td>
<td>23</td>
<td>48</td>
<td>extd0</td>
</tr>
<tr>
<td>16</td>
<td>d16</td>
<td>d48</td>
<td>24</td>
<td>49</td>
<td>extd8</td>
</tr>
<tr>
<td>17</td>
<td>d17</td>
<td>d49</td>
<td>25</td>
<td>50</td>
<td>extd1</td>
</tr>
<tr>
<td>18</td>
<td>d18</td>
<td>d50</td>
<td>26</td>
<td>51</td>
<td>extd9</td>
</tr>
<tr>
<td>19</td>
<td>d19</td>
<td>d51</td>
<td>27</td>
<td>52</td>
<td>extd2</td>
</tr>
<tr>
<td>20</td>
<td>d20</td>
<td>d52</td>
<td>28</td>
<td>53</td>
<td>extd10</td>
</tr>
<tr>
<td>21</td>
<td>d21</td>
<td>d53</td>
<td>29</td>
<td>54</td>
<td>extd11</td>
</tr>
<tr>
<td>22</td>
<td>d22</td>
<td>d54</td>
<td>30</td>
<td>55</td>
<td>extd12</td>
</tr>
<tr>
<td>23</td>
<td>d23</td>
<td>d55</td>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>d24</td>
<td>d56</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>d25</td>
<td>d57</td>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>d26</td>
<td>d58</td>
<td>34</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>d27</td>
<td>d59</td>
<td>35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>d28</td>
<td>d60</td>
<td>36</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>d29</td>
<td>d61</td>
<td>37</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>d30</td>
<td>d62</td>
<td>38</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>d31</td>
<td>d63</td>
<td>39</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>-</td>
<td>dok</td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>breq0</td>
<td>uok</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>breq1</td>
<td>brstn</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>breq2</td>
<td>brst1</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>breq3</td>
<td>brst0</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>frame</td>
<td>prstn</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>here</td>
<td>mclr</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>busy</td>
<td>cfgin</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>y0</td>
<td>y8</td>
<td>63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>y1</td>
<td>y9</td>
<td>62</td>
<td></td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>y2</td>
<td>y10</td>
<td>61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>y3</td>
<td>y11</td>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>y4</td>
<td>y12</td>
<td>59</td>
<td></td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>y5</td>
<td>y13</td>
<td>58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>y6</td>
<td>y14</td>
<td>57</td>
<td></td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>y7</td>
<td>y15</td>
<td>56</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Trace Example 2: Trace from SCI cable via SCILab’s SCITrac tracer

A SCITrac tracer must first be attached to the SCI cable. Two DT204.1 trace probes can be attached to the SCILab tracer as follows:

1. Trace probe 0:
   - E1 connects to pod1
   - E2 connects to pod2
   - EC connects to pod5

2. Trace probe 1:
   - E1 connects to pod3
   - E2 connects to pod4
   - EC not connected

3. An inter-probe cable must interconnect IPCON of trace probes 0 & 1.

4. The upstream JTAG daisy chain should be connected to JTAGIN of trace probe 0. A JTAG cable should interconnect JTAGOUT of trace probe 0 to JTAGIN of trace probe 1. The downstream chain should be connected to JTAGOUT of trace probe 1, but in the event of there being no downstream chain, its TDI should be strapped to its TDO.

5. Trace probes 0 & 1 must be connected via a DT205.1 probe adapter to deep trace board 0 & 1, respectively.

6. A synchronizing cable must interconnect J6 of probe adapters 0 & 1, respectively.

7. A trigger/trace cable must interconnect EXTCON of deep trace boards 0 & 1, respectively.

Then the straps must be selected as follows:

8. For both trace probes, the reference voltage must be selected via strap J22:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>J22 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>220mV</td>
<td>B-A</td>
</tr>
</tbody>
</table>

9. For trace probe 0, E1 must be selected as the clock source, and the IPCLK signal must be set up to output the selected clock to the other trace probe:

<table>
<thead>
<tr>
<th>Clock Source</th>
<th>J21 Straps</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1</td>
<td>E1-OUT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IPCLK</th>
<th>J11 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPCLK as output from CLKDVR</td>
<td>B-C</td>
</tr>
</tbody>
</table>

10. For trace probe 1, the clock source must come from IPCLK rather than E1, and the IPCLK signal must be set up to input the selected clock from the other trace probe:
Functional Overview

<table>
<thead>
<tr>
<th>Clock Source</th>
<th>J21 Straps</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPCLK</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IPCLK as input to CLKDVR</th>
<th>J11 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPCLK</td>
<td>B-A</td>
</tr>
</tbody>
</table>

11. For trace probe 0, the C7-0 must be strapped to register REG4, and C15-8 must be strapped to the inter-probe connector:

<table>
<thead>
<tr>
<th>Control Signals</th>
<th>Register Strap</th>
<th>Inter-probe Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>C7-0 to register</td>
<td>J3-10 C-D</td>
<td>J3-10 B-E</td>
</tr>
<tr>
<td>C15-8 to IP7-0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

12. For trace probe 1, the IP7-0 must be strapped to the register:

<table>
<thead>
<tr>
<th>Control Signals</th>
<th>Register Strap</th>
<th>Inter-probe Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP7-0 to register</td>
<td>-</td>
<td>J3-10 A-B</td>
</tr>
</tbody>
</table>

13. Each trace probe is strapped to trace an appropriate 8bit field of the external data as follows:

<table>
<thead>
<tr>
<th>External Data</th>
<th>Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>extD7-0</td>
<td>J12-19 B-C</td>
</tr>
<tr>
<td>extD15-8</td>
<td>J12-19 B-A</td>
</tr>
</tbody>
</table>

14. For trace probe 0, TXSYN must be output to the inter-probe connector:

<table>
<thead>
<tr>
<th>TXSYN</th>
<th>J2 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>MACH445 generates IPSYN</td>
<td>B-C</td>
</tr>
</tbody>
</table>

15. For trace probe 1, IPSYN must be treated as an input:

<table>
<thead>
<tr>
<th>TXSYN</th>
<th>J2 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPSYN is an input</td>
<td>-</td>
</tr>
</tbody>
</table>

The aggregated sample data fields are then as follows:
### Functional Overview

<table>
<thead>
<tr>
<th>SDxx</th>
<th>SCLOCK</th>
<th>DT200 board 0</th>
<th>DT200 board 1</th>
<th>I/O no.</th>
<th>MACH445 board 0</th>
<th>MACH445 board 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>bcik</td>
<td>bcik</td>
<td>i0/clk0</td>
<td></td>
<td>i1/clk1</td>
<td>oscout</td>
</tr>
<tr>
<td>0</td>
<td>d0</td>
<td>d32</td>
<td>8</td>
<td></td>
<td>i2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>d1</td>
<td>d33</td>
<td>9</td>
<td></td>
<td>i3/clk2</td>
<td>extclk</td>
</tr>
<tr>
<td>2</td>
<td>d2</td>
<td>d34</td>
<td>10</td>
<td></td>
<td>i4/clk3</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>d3</td>
<td>d35</td>
<td>11</td>
<td></td>
<td>i5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>d4</td>
<td>d36</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>d5</td>
<td>d37</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>d6</td>
<td>d38</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>d7</td>
<td>d39</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>d8</td>
<td>d40</td>
<td>16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>d9</td>
<td>d41</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>d10</td>
<td>d42</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>d11</td>
<td>d43</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>d12</td>
<td>d44</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>d13</td>
<td>d45</td>
<td>21</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>d14</td>
<td>d46</td>
<td>22</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>d15</td>
<td>d47</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>d16</td>
<td>d48</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>d17</td>
<td>d49</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>d18</td>
<td>d50</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>d19</td>
<td>d51</td>
<td>27</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>d20</td>
<td>d52</td>
<td>28</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>d21</td>
<td>d53</td>
<td>29</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>d22</td>
<td>d54</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>d23</td>
<td>d55</td>
<td>31</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>d24</td>
<td>d56</td>
<td>32</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>d25</td>
<td>d57</td>
<td>33</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>d26</td>
<td>d58</td>
<td>34</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>d27</td>
<td>d59</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>d28</td>
<td>d60</td>
<td>36</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>d29</td>
<td>d61</td>
<td>37</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>d30</td>
<td>d62</td>
<td>38</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>d31</td>
<td>d63</td>
<td>39</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>s1(F)</td>
<td>qc0[3]</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>s2(F)</td>
<td>qc0[2]</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>s3(F)</td>
<td>qc0[1]</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>s4(F)</td>
<td>qc0[0]</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>qc[2]</td>
<td>sync</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>qc[1]</td>
<td>L1[1]</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>qc[0]</td>
<td>L1[0]</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>y0</td>
<td>y8</td>
<td>63</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>y1</td>
<td>y9</td>
<td>62</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>y2</td>
<td>y10</td>
<td>61</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>y3</td>
<td>y11</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>y4</td>
<td>y12</td>
<td>59</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>y5</td>
<td>y13</td>
<td>58</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>y6</td>
<td>y14</td>
<td>57</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>y7</td>
<td>y15</td>
<td>56</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Functional Overview
**Electrical Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum sample data logical 1 input voltage</td>
<td>240 mVolts</td>
</tr>
<tr>
<td>Maximum sample data logical 1 input voltage</td>
<td>550 mVolts</td>
</tr>
<tr>
<td>Minimum sample data logical 0 input voltage</td>
<td>-50 mVolts</td>
</tr>
<tr>
<td>Maximum sample data logical 0 input voltage</td>
<td>80 mVolts</td>
</tr>
<tr>
<td>Resistive loading per input under test</td>
<td>390 ohms</td>
</tr>
<tr>
<td>Capacitive loading per input under test</td>
<td>5pF</td>
</tr>
<tr>
<td>Minimum TTL logical 1 input voltage</td>
<td>2.0 Volts</td>
</tr>
<tr>
<td>Maximum TTL logical 1 input voltage</td>
<td>5.5 Volts</td>
</tr>
<tr>
<td>Minimum TTL logical 0 input voltage</td>
<td>-0.5 Volts</td>
</tr>
<tr>
<td>Maximum TTL logical 0 input voltage</td>
<td>0.8 Volts</td>
</tr>
<tr>
<td>Minimum E1 clock frequency</td>
<td>0 Hz</td>
</tr>
<tr>
<td>Maximum E1 clock frequency</td>
<td>66 MHz</td>
</tr>
<tr>
<td>Minimum E1 clock logical 0 duration</td>
<td>5 nS</td>
</tr>
<tr>
<td>Minimum E1 clock logical 1 duration</td>
<td>5 nS</td>
</tr>
<tr>
<td>D[0..31] setup time relative to E1 clock positive transition</td>
<td>5 nS</td>
</tr>
<tr>
<td>D[0..31] hold time relative to E1 clock positive transition</td>
<td>1 nS</td>
</tr>
<tr>
<td>C[0..15] setup time relative to E1 clock positive transition</td>
<td>5 nS</td>
</tr>
<tr>
<td>C[0..15] hold time relative to E1 clock positive transition</td>
<td>1 nS</td>
</tr>
<tr>
<td>extD[0..15] setup time relative to extCLK positive transition</td>
<td>5 nS</td>
</tr>
<tr>
<td>extD[0..15] hold time relative to extCLK positive transition</td>
<td>1 nS</td>
</tr>
<tr>
<td>Supply current</td>
<td>TBD</td>
</tr>
</tbody>
</table>
### Functional Overview

#### Parts List

The parts list is:

<table>
<thead>
<tr>
<th>Part No</th>
<th>Supplier</th>
<th>Description</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>DT2041</td>
<td>ECS</td>
<td>PCB</td>
<td>1</td>
</tr>
<tr>
<td>BUF0-7</td>
<td>NatSemi DS92L90A EBV</td>
<td>LVDS tranceiver</td>
<td>8</td>
</tr>
<tr>
<td>TX0-1</td>
<td>NatSemi DS90C283 EBV</td>
<td>LVDS multiplexer</td>
<td>2</td>
</tr>
<tr>
<td>MACH445</td>
<td>AMD M4LV-128/64-7YC Lyco</td>
<td>MACH445 GAL</td>
<td>1</td>
</tr>
<tr>
<td>CLKDVR</td>
<td>TI CDC340</td>
<td>Farnell 149-230 (NEWK4063)</td>
<td>2</td>
</tr>
<tr>
<td>OSCDVR</td>
<td>TI SN74ABT646 Farnell 204250</td>
<td>8bit registers</td>
<td>5</td>
</tr>
<tr>
<td>OSOC</td>
<td>IQD 100MHz oscillator</td>
<td>100MHz 8pin oscillator</td>
<td>1</td>
</tr>
<tr>
<td>F1-1</td>
<td>SMD Filter Radionics CNF41</td>
<td>3-terminal bypass filter</td>
<td>16</td>
</tr>
<tr>
<td>C92</td>
<td>axial capacitor Farnell 430-870</td>
<td>0.1uF axial capacitor</td>
<td>2</td>
</tr>
<tr>
<td>C25-27</td>
<td>SMD tantalum capacitor Farnell 197-130</td>
<td>10uF 10V 1206 capacitor</td>
<td>10</td>
</tr>
<tr>
<td>C35</td>
<td>C45</td>
<td>C62</td>
<td>C75</td>
</tr>
<tr>
<td>C77</td>
<td>C82</td>
<td>axial capacitor</td>
<td>Farnell 430-870</td>
</tr>
<tr>
<td>C20-24</td>
<td>C28-30</td>
<td>C34</td>
<td>C54</td>
</tr>
<tr>
<td>C63</td>
<td>C73</td>
<td>C78-85</td>
<td>C87-89</td>
</tr>
<tr>
<td>C91</td>
<td>C92</td>
<td>SMD capacitor</td>
<td>Farnell 317-640</td>
</tr>
<tr>
<td>C71</td>
<td>ceramic capacitor</td>
<td>Farnell 286-930</td>
<td>100pF capacitor</td>
</tr>
<tr>
<td>C72</td>
<td>tantalum capacitor</td>
<td>Farnell 643-701</td>
<td>22uf 16V capacitor</td>
</tr>
<tr>
<td>C6-19</td>
<td>C31-33</td>
<td>C36-44</td>
<td>C46-52</td>
</tr>
<tr>
<td>C55-61</td>
<td>C64-70</td>
<td>C93-95</td>
<td>C100-103</td>
</tr>
<tr>
<td>C105-138</td>
<td>SMD capacitor</td>
<td>Farnell 499-146</td>
<td>0.01uF 10% 0603 capacitor</td>
</tr>
<tr>
<td>C1-5</td>
<td>C20-42</td>
<td>C28-30</td>
<td>C34</td>
</tr>
<tr>
<td>C54</td>
<td>C63</td>
<td>C73</td>
<td>C78-85</td>
</tr>
<tr>
<td>C87-89</td>
<td>C91</td>
<td>C92</td>
<td>SMD capacitor</td>
</tr>
<tr>
<td>C71</td>
<td>ceramic capacitor</td>
<td>Farnell 286-930</td>
<td>100pF capacitor</td>
</tr>
<tr>
<td>C72</td>
<td>tantalum capacitor</td>
<td>Farnell 643-701</td>
<td>22uf 16V capacitor</td>
</tr>
</tbody>
</table>
### Functional Overview

<table>
<thead>
<tr>
<th>Component</th>
<th>Type/Description</th>
<th>Brand/Code</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>C6-19</td>
<td>SMD capacitor</td>
<td>Farnell 578-174</td>
<td>0.022uF 10% 0603 capacitor</td>
</tr>
<tr>
<td>C31-33</td>
<td>SMD capacitor</td>
<td>Farnell 317-275</td>
<td>0.47uF 80% 0603 capacitor</td>
</tr>
<tr>
<td>C36-44</td>
<td>SMD capacitor</td>
<td>Farnell 911-185</td>
<td>390ohm 1% 0603 resistor</td>
</tr>
<tr>
<td>C46-52</td>
<td>SMD capacitor</td>
<td>Farnell 911-318</td>
<td>4.7Kohm 1% 0603 resistor</td>
</tr>
<tr>
<td>C55-61</td>
<td>SMD capacitor</td>
<td>Farnell 514-184</td>
<td>4.7Kohm 10% resistor</td>
</tr>
<tr>
<td>C64-70</td>
<td>Metal film resistor</td>
<td>Farnell 513-623</td>
<td>220ohm 10% resistor</td>
</tr>
<tr>
<td>C93-95</td>
<td>Metal film resistor</td>
<td>Farnell 513-866</td>
<td>220ohm 10% resistor</td>
</tr>
<tr>
<td>C100-103</td>
<td>Metal film resistor</td>
<td>Farnell 513-908</td>
<td>330ohm 10% resistor</td>
</tr>
<tr>
<td>C105-138</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>T1-54</td>
<td>SMD capacitor</td>
<td>Farnell 513-906</td>
<td>220ohm 10% resistor</td>
</tr>
<tr>
<td>R1-8</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R9</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R12-18</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R19-25</td>
<td>Metal film resistor</td>
<td>Farnell 513-908</td>
<td>330ohm 10% resistor</td>
</tr>
<tr>
<td>R29</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R30</td>
<td>Metal film resistor</td>
<td>Farnell 513-908</td>
<td>330ohm 10% resistor</td>
</tr>
<tr>
<td>R31-32</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R35</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R36</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R37</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R38</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R39</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R40</td>
<td>Metal film resistor</td>
<td>Farnell</td>
<td>?ohm 10% resistor</td>
</tr>
<tr>
<td>R27-28</td>
<td>SIP resistor</td>
<td>Farnell 106-466</td>
<td>220/330ohm 16 resistors</td>
</tr>
<tr>
<td>R10-11</td>
<td>SIP resistor</td>
<td>Farnell 148-983</td>
<td>4.7Kohm 8 resistors</td>
</tr>
<tr>
<td>VREG1-2</td>
<td>NatSemi LM39401T-3.3</td>
<td>Farnell 412-132</td>
<td>3.3V voltage regulator</td>
</tr>
<tr>
<td>PWRLED</td>
<td>LED</td>
<td>Farnell 595-524</td>
<td>Wide angle LED</td>
</tr>
<tr>
<td>GND1-6</td>
<td>Ground pins</td>
<td>Farnell 329-551</td>
<td>Test point pins</td>
</tr>
<tr>
<td>J1-22</td>
<td>strap block</td>
<td>Farnell 312-230</td>
<td>32pin strap block</td>
</tr>
<tr>
<td>PWRCON1</td>
<td>Socket</td>
<td>Farnell 588-738</td>
<td>4pin right angle socket</td>
</tr>
<tr>
<td>PWRCON2</td>
<td>Socket</td>
<td>Farnell 588-910</td>
<td>4pin right angle socket</td>
</tr>
<tr>
<td>LVDSCON</td>
<td>Socket</td>
<td>Farnell 972-605</td>
<td>34pin right angle socket</td>
</tr>
<tr>
<td>XTLCOR</td>
<td>Socket</td>
<td>Farnell 468-885</td>
<td>10pin socket</td>
</tr>
<tr>
<td>E1-2</td>
<td>Socket</td>
<td>Farnell 468-915</td>
<td>20pin socket</td>
</tr>
<tr>
<td>EXTCON</td>
<td>Socket</td>
<td>Farnell 468-892</td>
<td>40pin socket</td>
</tr>
<tr>
<td>NSCON0-1</td>
<td>Socket</td>
<td>Farnell 468-952</td>
<td>50pin socket</td>
</tr>
</tbody>
</table>

---

Page 24 30th March, 1999
Trace Probe DT204.1

Patch List

1. Surface Wire Patches
   1.1 none so far.

2. Internal Trace Patches
   2.1 none so far.

3. Remaining Problems
   3.1 none so far.

4. Major Recent Fixes
   4.1 dd-MMM-yyyy : none so far.

5. Still to be Done
   5.1 Need to buffer the external interface so that it can be disabled with the JTAG /ENABLE signal to allow in-circuit programming of the MACH445 even when an external source is connected.

2. Discontinued following decision to switch to designing DT203.1 trace probe for direct attachment to Dolphin D310 SCI board B-Link pads.

3. Revived and revised following Dassault's comments at Berlin meeting 17-MAR-1999, requiring attachment to Hewlett Packard HP1600 series probe sockets as per Dolphin's probe card. Changed to use DS90C283/DS90C284 in same way as DT203.1, since DS90C387/DS90CF388 development is delayed.

4. Revised following discussion with Bernhard Skaali 30-MAR-1999, to provide for attachment to SCILab tracer. DT200.1 database definitions also changed to match.

5. 18-MAY-1999 : TXSYN is on 25th bit, not 28th bit.
Probe Adapter DT205.1

Technical Manual
Introduction

The DT205.1 Probe Adapter allows simple attachment of the DT200.1 Deep Tracer to trace probes for IEEE 1596 Scalable Coherent Interconnect (SCI) systems. Two trace probes and probe adapters are needed, one pair of each to attach to each one of the two deep trace boards.

Features

- Simple deep tracer interface
  34-way LVDS cable.

- 48bit trace data samples
  Max Sample Rate 66MHz.

- Synchronizing buffer
  +/-25nS skew tolerance.
Functional Overview

Probe Adapter Functional Overview

A simplified schematic of the probe adapter is shown below.

Each probe adapter attaches to 48 bits of a 96-bit sample data path. A flat 34-way cable (typically a floppy-disk cable), carrying eight differential signals plus two differential clocks, connects the LVDS inputs to J1 on the probe adapter at the deep trace board. The cable pinout is as follows:

<table>
<thead>
<tr>
<th>Left</th>
<th>Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx0OUT0M</td>
<td>Tx0OUT0P</td>
</tr>
<tr>
<td>AGND</td>
<td>AGND</td>
</tr>
<tr>
<td>TX0OUT1M</td>
<td>Tx0OUT1P</td>
</tr>
<tr>
<td>AGND</td>
<td>Tx0OUT3M</td>
</tr>
<tr>
<td>Tx0OUT3P</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx0OUT2M</td>
<td>Tx0OUT2P</td>
</tr>
<tr>
<td>AGND</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx0CLKM</td>
<td>Tx0CLKP</td>
</tr>
<tr>
<td>N.C.</td>
<td>N.C.</td>
</tr>
<tr>
<td>Tx1OUT0M</td>
<td>Tx1OUT0P</td>
</tr>
<tr>
<td>AGND</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx1OUT1M</td>
<td>Tx1OUT1P</td>
</tr>
<tr>
<td>AGND</td>
<td>Tx1OUT3M</td>
</tr>
<tr>
<td>Tx1OUT3P</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx1OUT2M</td>
<td>Tx1OUT2P</td>
</tr>
<tr>
<td>AGND</td>
<td>AGND</td>
</tr>
<tr>
<td>Tx1CLKM</td>
<td>Tx1CLKP</td>
</tr>
</tbody>
</table>

Two probe adapters are synchronized via a cable that connects to J6, which has the following pinout:

<table>
<thead>
<tr>
<th>Left</th>
<th>Right</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>SCLOCKIN</td>
</tr>
<tr>
<td>GND</td>
<td>SDSYN</td>
</tr>
<tr>
<td>GND</td>
<td>RDADR[0]</td>
</tr>
<tr>
<td>GND</td>
<td>RDADR[1]</td>
</tr>
<tr>
<td>GND</td>
<td>N.C.</td>
</tr>
</tbody>
</table>
The LVDS data signals are parallel terminated by 100 ohms across each differential pair. These multiplexed LVDS signals are then demultiplexed using two DS90C284 devices, IC2 for the low 24bits, and IC1 for the high 24bits. Each generates a 28bit demultiplexed low voltage TTL data output, representing a 24bit trace sample stream plus four control signals.

Since the data from different devices may be skewed (relative to each other) at the end of the LVDS cables, a synchronizing pulse RXSYN is received over the 25th output bit; which repeats every 3 clock cycles. This is used to synchronize the four 24bit trace sample streams over two probe adapters into one synchronous 96bit stream.

The synchronizer is programmed into two MACH445 pals, IC4 for the low 24bits and IC3 for the high 24bits. These create a three-stage buffer that is written to by the DS90C284, and read from by the deep tracer. A buffer write address counter is clocked from the DS90C284, but is reset every 3 cycles by the synchronizing pulse. Three stages allow a LVDS skew tolerance of +/-25nS, more than twice the minimum margin for a DS90C284 at 66MHz.

A delayed clock and synchronizing pulse are generated by the delay lines IC6 and IC7; these are fed to each MACH445 pal on a probe adapter. One of the four MACH445 pals of a pair of probe adapters is selected as master via strap J7 as follows:

<table>
<thead>
<tr>
<th>Role</th>
<th>J7 Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Master</td>
<td>A-B</td>
</tr>
<tr>
<td>Slave</td>
<td>-</td>
</tr>
</tbody>
</table>

The master then generates a read clock and synchronizing pulse, and uses these to clock and reset a buffer read address counter. From this it generates read address outputs, which are used by all four MACH445 pals to read the buffer. The clock, synchronizing pulse and read address signals are distributed over the two probe adapters via the synchronizing cable.

The MACH445 pal can also be used as a test pattern generator. It may be programmed via a JTAG interface using the MACHXL software.

The MACH445 pal can further be employed to match specific input data patterns, again programmed via the JTAG interface using the MACHXL software. The match results can be pipelined to the tracer via the control fields.

Two JTAG connectors are provided. The upstream of the JTAG chain connects to J3, and the downstream connects to J4. Their pin connections are:

<table>
<thead>
<tr>
<th>TCK</th>
<th>ZCTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMS</td>
<td>GND</td>
</tr>
<tr>
<td>TDI</td>
<td>TVCC</td>
</tr>
<tr>
<td>TDO</td>
<td>GND</td>
</tr>
<tr>
<td>/TRST</td>
<td>ENABLE</td>
</tr>
</tbody>
</table>

In the event that there is no downstream chain, TDI should be strapped to TDO at connector J4. Note that signals /TRST, /ENABLE and TVCC are resistively pulled up to 5V, while signal ZCTL is resistively pulled down to ground.

Strap J8 can be shorted to power down the DS90C284 devices.
5V power is normally obtained from J2, but for standalone debugging it can be supplied via J5. A 3.3V voltage regulator then generates 3.3V for the DS90C284 and MACH445 devices. There are three internal PCB power planes: +5V, +3.3V and ground. The DS90C284 devices have isolated power and grounds for both the LVDS interfaces and their phase-lock loops; power is isolated via filters while ground is isolated via trace inductances.

The MACH445 pals output the 48bit sample stream to the deep tracer via J2. A CDC340 clock driver buffers the clock to drive the deep tracer. The pinout of J2 board (from the component side of the connector) is as follows:
| 1 | SCLOCKIN | GND | GND | D23 | GND | D47 |
| GND | D22 | GND | D46 |
| GND | D21 | GND | D45 |
| GND | D20 | GND | D44 |
| GND | D19 | GND | D43 |
| GND | D18 | GND | D42 |
| GND | D17 | GND | D41 |
| GND | D16 | GND | D40 |
| GND | D15 | GND | D39 |
| GND | D14 | GND | D38 |
| GND | D13 | GND | D37 |
| GND | D12 | GND | D36 |
| GND | D11 | GND | D35 |
| GND | D10 | GND | D34 |
| GND | D9 | GND | D33 |
| GND | D8 | GND | D32 |
| GND | D7 | GND | D31 |
| GND | D6 | GND | D30 |
| GND | D5 | GND | D29 |
| GND | D4 | GND | D28 |
| GND | D3 | GND | D27 |
| GND | D2 | GND | D26 |
| GND | D1 | GND | D25 |
Functional Overview
## Functional Overview

### Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>minimum logical 1 input voltage</td>
<td>2.0 Volts</td>
</tr>
<tr>
<td>maximum logical 1 input voltage</td>
<td>5.5 Volts</td>
</tr>
<tr>
<td>minimum logical 0 input voltage</td>
<td>-0.5 Volts</td>
</tr>
<tr>
<td>maximum logical 0 input voltage</td>
<td>0.8 Volts</td>
</tr>
<tr>
<td>capacitive loading per input under test</td>
<td>TBD</td>
</tr>
<tr>
<td>minimum SCLOCKIN frequency</td>
<td>0 Hz</td>
</tr>
<tr>
<td>maximum SCLOCKIN frequency</td>
<td>66 MHz</td>
</tr>
<tr>
<td>minimum SCLOCKIN logical 0 duration</td>
<td>5 nS</td>
</tr>
<tr>
<td>minimum SCLOCKIN logical 1 duration</td>
<td>5 nS</td>
</tr>
<tr>
<td>SD[0..47] setup time relative to SCLOCKIN positive transition</td>
<td>5 nS</td>
</tr>
<tr>
<td>SD[0..47] hold time relative to SCLOCKIN positive transition</td>
<td>1 nS</td>
</tr>
<tr>
<td>supply current</td>
<td>TBD</td>
</tr>
</tbody>
</table>
### Parts List

The parts list is:

<table>
<thead>
<tr>
<th>No.</th>
<th>Part No</th>
<th>Supplier</th>
<th>Description</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>DT2051</td>
<td>ECS</td>
<td>PCB</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>IC1</td>
<td>NatSemi DS90C284</td>
<td>EBV</td>
<td>LVDS demultiplexer</td>
<td>2</td>
</tr>
<tr>
<td>IC2</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>IC3</td>
<td>AMD M4LV-128/64-7YC</td>
<td>Lyco</td>
<td>MACH445 GAL</td>
<td>2</td>
</tr>
<tr>
<td>IC4</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>IC5</td>
<td>TI CDC340</td>
<td>Farnell 149-230 (NEWK4063)</td>
<td>Clock driver</td>
<td>1</td>
</tr>
<tr>
<td>IC6</td>
<td>Newport 50A10250</td>
<td>Farnell 203-208</td>
<td>25ns Delay line</td>
<td>2</td>
</tr>
<tr>
<td>IC7</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>XOSC</td>
<td>IQD 100MHz oscillator</td>
<td>Farnell 101-412</td>
<td>100MHz 14pin oscillator</td>
<td>1</td>
</tr>
<tr>
<td>F1-4</td>
<td>SMD Filter</td>
<td>Radionics CNF41</td>
<td>3-terminal bypass filter</td>
<td>4</td>
</tr>
<tr>
<td>C58</td>
<td>ceramic capacitor</td>
<td>Farnell 286-930</td>
<td>100pF capacitor</td>
<td>1</td>
</tr>
<tr>
<td>C59</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C1-5</td>
<td>SMD capacitor</td>
<td>Farnell 317-640</td>
<td>1uF 10% 0805 capacitor</td>
<td>25</td>
</tr>
<tr>
<td>C16-17</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C23</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C32</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C35</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C38</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C41-45</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C47-55</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C75-78</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C46</td>
<td>tantalum capacitor</td>
<td>Farnell 643-701</td>
<td>22uF/16V capacitor</td>
<td>1</td>
</tr>
<tr>
<td>C6-15</td>
<td>SMD capacitor</td>
<td>Farnell 499-146</td>
<td>0.01uF 10% 0603 capacitor</td>
<td>31</td>
</tr>
<tr>
<td>C18-22</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C24-31</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C33-34</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C36-40</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C100</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C101</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C61-74</td>
<td>SMD capacitor</td>
<td>Farnell 578-174</td>
<td>0.022uF 10% 0603 capacitor</td>
<td>34</td>
</tr>
<tr>
<td>C18-22</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C24-31</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C33-34</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C36-40</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C56-57</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>C60</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>R9-12</td>
<td>Metal film resistor</td>
<td>Farnell 514-184</td>
<td>4.7Kohm 10% resistor</td>
<td>6</td>
</tr>
<tr>
<td>R14-15</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>R24-33</td>
<td>SMD resistor</td>
<td>Farnell 911-112</td>
<td>100ohm 1% 0603 resistor</td>
<td>10</td>
</tr>
<tr>
<td>R13</td>
<td>SMD resistor</td>
<td>Farnell 911-033</td>
<td>22ohm 1% 0603 resistor</td>
<td>9</td>
</tr>
<tr>
<td>R16-20</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>R22-23</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>R34</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>R21</td>
<td>SMD resistor</td>
<td>Farnell 911-239</td>
<td>1kohm 1% 0603 resistor</td>
<td>1</td>
</tr>
<tr>
<td>VR1</td>
<td>NatSemi LM39401T-3.3</td>
<td>Farnell 412-132</td>
<td>3.3V voltage regulator</td>
<td>1</td>
</tr>
<tr>
<td>J7</td>
<td>strap block</td>
<td>Farnell 312-230</td>
<td>32pin strap block</td>
<td>1</td>
</tr>
</tbody>
</table>
## Functional Overview

<table>
<thead>
<tr>
<th>J5</th>
<th>Socket cable plug</th>
<th>Farnell 588-738</th>
<th>Farnell 588-910</th>
<th>4pin right angle socket</th>
<th>4pin cable plug</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Socket cable plug</td>
<td>Farnell 972-605</td>
<td>Farnell 525-418</td>
<td>Farnell 296-879</td>
<td>34pin right angle socket</td>
<td>34pin flat cable plug</td>
</tr>
<tr>
<td>J3-4</td>
<td>Socket cable plug</td>
<td>Farnell 468-885</td>
<td>Farnell 525-364</td>
<td>Farnell 296-806</td>
<td>10pin socket</td>
<td>30metres 10pin flat cable plug</td>
</tr>
<tr>
<td>J6</td>
<td>Socket cable plug</td>
<td>Farnell 468-885</td>
<td>Farnell 525-364</td>
<td>Farnell 296-806</td>
<td>10pin socket</td>
<td>30metres 10pin flat cable plug</td>
</tr>
<tr>
<td>J2</td>
<td>plug</td>
<td>AMP 749084-9</td>
<td></td>
<td></td>
<td>100pin right angle plug</td>
<td>1</td>
</tr>
</tbody>
</table>
1. Surface Wire Patches
   1.1 none so far.

2. Internal Trace Patches
   2.1 none so far.

3. Remaining Problems
   3.1 none so far.

4. Major Recent Fixes
   4.1 dd-MMM-yyyy : none so far.

5. Still to be Done
   5.1 none so far.
Probe Adapter DT205.1

Document History


2. 18-MAY-1999: added layouts, updated J1 pinout, and RXSYN is on 25\text{th} bit, not 28\text{th} bit.